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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | | ATTORNEY DOCKET NO. |
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| 09/217,401 | 12/21/98 | ISHIDA | K | 884.088US1 |

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| **ART UNIT** | **PAPER NUMBER** |
| 2841 | |

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**DATE MAILED:** 07/18/00

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/217,401 | ISHIDA ET AL. | |
| | Examiner | Art Unit | |
| | Thanh Y. Tran | 2841 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

**Status**

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/21/98* is/are objected to by the Examiner.

11)☒ The proposed drawing correction filed on *12/21/98* is: a)☒ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

**Attachment(s)**

15)☒ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other: .

## DETAILED ACTION

### *Drawings*

The drawings are objected to because the specification discloses at pages 4-7, that "socket 104" relates to the drawings in Figs. 1-2, therefore, Figs. 1 and 2 need to be labeled the drawing's numbers as mentioned in specification. Correction is required.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Allen et al. (U.S. 4,705,205).

As to claim 1, Allen et al. discloses a mounting socket (see Figs. 7 & 10, and col. 16, lines 60-68), comprising:

a socket body having a first side and a second, opposite side (see Fig. 7, elements 32 & 34), the body having a plurality of vias ("holes") extending therethrough (see Fig. 7, "holes-36" or "holes-38"; and col. 16, lines 60-68); a plurality of conductive terminals (see Fig. 7, elements 28) within the vias (36 or 38) (see col. 16, lines 60-68) wherein the terminals (28) comprise: an elastically deformable member (see Figs. 3(B) & 13, element 18 or 62; and col. 9, lines 45-65, also col. 12, lines 3-8).

As to claim 2, Allen et al. discloses the mounting socket (see Figs. 7 & 13) wherein the elastically deformable member (see Fig. 3(B), element 18) comprises a spring (see Fig. 13, "spring-62"; and col. 19, lines 10-26).

As to claim 3, Allen et al. discloses the mounting socket (see Figs. 3(B), 7 & 13) wherein the elastically deformable member (18 or 28) comprises a dish spring ("coil") (see Fig. 13, "spring-62" or col. 19, lines 10-26).

As to claim 4, Allen et al. discloses the mounting socket (see Figs. 3(B), 7 & 13) wherein the elastically deformable member (18 or 28) comprises: a coil (Fig. 13, element 62; or col. 19, lines 10-26); and a conductive polymer ("plastic" or "polymeric material") (see Fig. 3(B), col. 9, lines 45-60, and col. 13, lines 20-33) injected within the vias ("holes") (see Fig. 7, elements 36, 38 & 39; and col. 12, lines 35-58).

As to claim 5, Allen et al. discloses the mounting socket (see Fig. 7 & 10) further comprising: a first adhesive layer affixed to the first side of the body (see Fig. 10, and col. 17, lines 32-62).

As to claim 6, Allen et al. discloses the mounting socket (see Figs. 7 & 10) further comprising: a polymer tape ("polymeric material" or "plastic") (see col. 9, lines 45-60, and col. 13, lines 20-33) applied to the first adhesive layer (see Fig. 10, and col. 17, lines 32-62); a ground and power line circuit laid on the polymer tape (see Fig. 10; or col. 3, lines 17-35, col. 8, line 62 - col. 9, line 20, col. 13, lines 20-33; also col. 14, lines 24-38); and a second adhesive layer (46) (see Figs. 9 & 10, col. 17, line 32- col. 18, line 15) applied on and protecting the ground and power line circuit.

As to claim 7, Allen et al. discloses the mounting socket (see Figs. 7 & 10) further comprising: a second adhesive layer (46) affixed to the second side of the body (see Fig. 10, element 34).

As to claim 8, Allen et al. discloses the mounting socket (see Figs. 7 & 10) further comprising: a push cover attachable to the socket body first and second sides (see Figs. 9 & 10, elements 32 & 34; and col. 17, lines 32-62, also col. 20, lines 50-60).

As to claim 9, Allen et al. teaches a method of mounting a socket (see Figs. 7 & 10, elements 32 & 34) to a board, comprising: applying an adhesive layer to a board side of the socket (see Fig. 10, "adhesive-46"; col. 17, lines 32-62, and col. 20, lines 50-60); leveling the adhesive layer (46) to make the adhesive layer substantially coplanar with contact terminals of the socket (see Fig. 10); and adhering the socket (32) to the board (34) (see Fig. 10, col. 17, lines 32-62, and col. 20, lines 50-60).

As to claim 10, Allen et al. teaches the method further comprising: applying a second adhesive layer (see Fig 10, element 40 or 46) to a package side of the socket (32) opposite the board side (34) of the socket; and adhering a package (32) to the second adhesive layer (40 or 46) (see Fig. 10, col. 17, lines 32- col. 18, lines 15, and col. 20, lines 50-60).

As to claim 11, Allen et al. teaches a method of mounting a package to a board (see Figs. 7, 8 & 10) using a socket (32) having contact terminals (10), the method comprising:

applying a first adhesive layer to a first, package side of the socket (32) (see Fig. 10, col. 17, lines 32-62, and col. 20, lines 50-60); leveling the first adhesive layer to make the adhesive layer substantially coplanar with the contact terminals (see Fig. 10); adhering the package to the first adhesive layer (see Fig. 7 & 10, col. 17, lines 32-62, and col. 20, lines 50-60);

applying a second adhesive layer (see Fig. 10, element 40 or 46) to a second, board side of the socket (34); leveling the second adhesive layer (40 or 46) to make the second adhesive layer substantially coplanar with the contact terminals (see Fig. 10); and adhering the board (34) to the second adhesive layer (46) (see Figs. 7 & 10, col. 17, line 32 - col. 18, line 15, and col. 20, lines 50-60).

As to claim 12, Allen et al. discloses a circuit interconnect (see Figs. 4, 7 & 10), comprising: a circuit board carrier (32 or 34) having a plurality of through holes ("holes-36" or "holes-38") formed therein; and a plurality of conductive terminals (see Fig. 7, element 28) with lands (10 or 12) at each end, each terminal (28) in one of the through holes (36 or 38), wherein each conductive terminal (see element 18 in Fig. 3(B), or element 28 in Fig. 7) comprises an elastically deformable member (see Figs. 3(B) & 13, element 18 or 62; and col. 9, lines 45-65; col. 12, lines 3-8; col. 16, lines 52-68; and col. 19, lines 10-26).

As to claim 13, Allen et al. discloses the circuit interconnect (see Figs. 4, 7 & 10) further comprising: a first adhesive layer affixed to a first side of the circuit board carrier (32) (see Fig. 10, and col. 17, lines 32-62), the first layer having openings ("holes-36") (see Figs. 7, 9 & 10) to expose the lands (10).

As to claim 14, Allen et al. discloses the circuit interconnect (see Figs. 4, 7 & 10) further comprising: a second adhesive layer (see Fig. 10, element 46) affixed to a second side of the circuit board carrier (34), the second layer (46) having openings ("holes-38") (see Fig. 7, "holes-38") to expose the lands (12), the second side opposite the first side (see Figs. 7 & 10, elements 32 & 34).

As to claim 15, Allen et al. discloses the circuit interconnect (see Figs. 3(B), 4 & 8) wherein the conductive terminals (18 or 28) are conductive rubber ("plastic") (see col. 9, lines 45-60).

As to claim 16, Allen et al. discloses the circuit interconnect (see Figs. 3(B) & 13) wherein the conductive terminals (see Fig. 3(B), element 18) comprise a spring (62) (see Fig. 13, and col. 19, lines 10-26).

As to claim 17, Allen et al. discloses the circuit interconnect (see Figs. 3(B), 7 & 13) wherein the conductive terminals (18 or 28) comprise: a compressible coil (62) (see Fig. 13, col. 19, lines 10-26); and a conductive polymer ("plastic" or "polymeric material") (see col. 9, lines 45-60, col. 10, lines 27-40, and col. 13, lines 20-35) injected within the vias ("holes") (see Fig. 7, holes 36 or 38 or 39)

As to claim 18, Allen et al. discloses a circuit package (see Figs. 7 & 10), comprising: a substrate (34) having a plurality of conductive terminals (28) therethrough; a first adhesive layer (see Fig. 10) affixed to a first side of the substrate (32); and a package (32) affixed to the first adhesive layer (see Fig. 10, col. 17, lines 32-62).

As to claim 19, Allen et al. discloses the circuit package (see Figs. 7 & 10) further comprising: a second adhesive layer (see Fig. 10, element 46) affixed to a second side of the substrate (34), the second side opposite the first side (32) (see Fig. 10, col. 17, lines 32-62).

As to claim 20, Allen et al. discloses an integrated circuit (see Figs. 7 & 10), comprising: a substrate (34) having a plurality of vias ("holes") (38) therein; and a plurality of elastically deformable terminals (28), each terminal positioned in a via ("hole-38").

As to claim 21, Allen et al. discloses a circuit assembly (see Figs. 7 & 10), comprising: a substrate (34) having a built-in socket, the socket (32) having a plurality of vias ("holes-36") therein; a plurality of elastically deformable, conductive terminals (see element 28 in Fig. 7 or 18 in Fig. 3(B); also col. 9, lines 45-60), each terminal (18 or 28) within a via (36 or 38); a circuit board (34) having a plurality of mounting areas (10 & 12), the mounting areas (10 & 12) in a plurality of planes (22) which are substantially non-planar with each other; and wherein each terminal (28) is individually deformable to contact its respective mounting area (10 & 12) at the plane of the mounting area (see col. 16, lines 52 - col. 17, line 5 & lines 48-62).

As to claim 22, Allen et al. discloses a circuit assembly (see Figs. 7 & 10), comprising: a microprocessor (chip carrier-32); a substrate (34) having a built-in socket having a plurality of vias ("holes") (36 or 38) therein, and a plurality of conductive, elastically deformable terminals (see element 28 in Fig. 7 or 18 in Fig. 3(B)), at least a portion of the plurality of terminals (see Fig. 3 (B) &10, element 18 or 28) within a via (36 or 38); and a motherboard (see Fig. 10, "circuit board-34") having a plurality of mounting areas (12) thereon, each elastically deformable terminal (see element 18 in Fig. 3(B), or 28 in Fig. 7), deformed to contact a mounting area (12) (see Fig. 7 & 13, col. 9, lines 45-60, and col. 19, lines 10-26).

## *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Allen et al. (U.S. 4,705,205) teaches "Chip carrier mounting device".

## Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (703) 305-4757. The examiner can normally be reached on Monday through Thursday and on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeff Gaffin, can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-3431.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TYT